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Depositor: John A. Jordan

11/26/02
(Signature and Date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of :	November 26, 2002
Gregg J. Armezzani, et al. :	Examiner: J.B. Vigushin
Serial No.: 09/764,476 :	Art Unit: 2827
Filed: January 17, 2001 :	IBM Corporation Intellectual Property Law Dept. N50/040-4, 1701 North Street Endicott, New York 13760
Title: **ELECTRONIC PACKAGE WITH STACKED CONNECTIONS AND METHOD FOR MAKING SAME** :	

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Examiner's Office Action of October 2, 2002, please amend the application as follows:

In the Specification:

Page 6, line 18, change "benzatriazole" to --benzotriazole--.

In the Claims:

Please cancel Claims 32, 33, 38 - 43 and 45.

Please amend Claims 26, 34 and 44 as follows:

Claim 26. An electronic package comprising:

a first flexible circuitized substrate having at least one conductive aperture therein having an external surface;

a second flexible circuitized substrate having at least one conductive aperture therein having an external surface, said first and second flexible circuitized substrates aligned such that said at least one conductive aperture of said first flexible circuitized substrate is substantially aligned with said at least one conductive aperture of said second flexible circuitized substrate wherein said first and second flexible circuitized substrates are comprised of a material selected from the group consisting of polyimide, polytetrafluoro-ethylene, and epoxy glass cloth, said at least one conductive aperture of said first flexible circuitized substrate and said at least one conductive aperture of said second flexible circuitized substrate including a conductive metallic layer thereon selected from the group consisting of copper, nickel, gold, chromium, solder and alloys thereof; and

at least one solder member including a first contact portion extending from said external surface of said conductive aperture of said first flexible circuitized substrate and a second contact portion extending substantially within both of said aligned conductive apertures of said first and second flexible circuitized substrates to said external surface of said conductive aperture of said second flexible circuitized substrate so as to substantially form a solder dome thereon and secure said flexible circuitized substrates together.

Claim 34. The electronic package of Claim 26 wherein said second contact portion of said solder member including said solder dome is at least one of an array of

solder members on said external surface of said conductive aperture of said second flexible circuitized substrate.

Claim 44. A single chip carrier comprising:

a first circuitized substrate having at least one conductive aperture therein having an external surface;

a second circuitized substrate having at least one conductive aperture therein having an external surface, said first and second circuitized substrates aligned such that said at least one conductive aperture of said first circuitized substrate is substantially aligned with said at least one conductive aperture of said second circuitized substrate, said at least one conductive aperture of said first circuitized substrate and said at least one conductive aperture of said second circuitized substrate including a conductive metallic layer thereon selected from the group consisting of copper, nickel, gold, chromium, solder and alloys thereof;

at least one solder member including a first contact portion for connection to a printed circuit board extending from said external surface of said conductive aperture of said first circuitized substrate and a second contact portion extending substantially within both of said aligned conductive apertures of said first and second circuitized substrates to said external surface of said conductive aperture of said second circuitized substrate so as to substantially form a solder dome thereon to secure said circuitized substrates together wherein said second contact portion of said solder member is at least one of an array of solder members on said external surface of said conductive aperture of said second circuitized substrate; and

at least one chip attached to said array of solder members.

REMARKS

Claims 26 - 45 have been rejected by the Examiner. By this amendment, Claims 32, 33, 38 - 43 and 45 have been canceled and Claims 26, 34 and 44 have been amended.

THE 35 USC 112 REJECTION

The Examiner has rejected Claims 26 - 45 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In this regard the Examiner points to Applicants' specification (page 6) that describes the use of protective layers of benzotrozole, chlorite, or immersion tin in the context of the protection of copper. However, Applicants would like to point of that Applicants originally filed application, Serial No. 09/282,842 claimed these protective coatings as applicable to copper, nickel, gold, chromium, solder and alloys thereof.

However, in order to expedite prosecution Applicants have canceled that portion of each claim calling for these protective coatings. Accordingly, Applicants believe that by this action they have clearly overcome the Examiner's 35 USC 112 rejection.

THE 35 USC 102(a) REJECTION

The Examiner has further rejected Claims 38 - 41 and 43 - 45 under 35 USC 102(b) as being anticipated by Bindra, et al. Since Applicants have canceled Claims 38 - 43 and 45 only Claim 44 remains under this rejection. In this regard, Claim 44 has been amended to more clearly distinguish over Bindra, et al.

Bindra, et al are directed to a high performance printed circuit board arrangement comprising at least two circuitized power cores laminated together. Vias and lands are first opened in the power core structures and are filled with joining metal. The vias are then aligned and electrically connected to one another by dendrite connectors or solder, located between the joining metal within the aligned conductive vias.

DISTINCTIONS BETWEEN THE BINDRA, ET AL. TEACHINGS AND APPLICANTS' TEACHINGS

From the above brief description, it can be seen that the Bindra, et al. structure is not at all similar to that claimed by Applicants. Bindra, et al. is directed to encapsulated circuited power core alignment and lamination in the fabrication of printed circuit boards. Applicants' invention, on the other hand, is directed to a chip carrier structure that employs conductive vias filled with one contiguous solder member to electrically connect and mechanically secure together two flexible circuitized substrates. The solder member unites aligned conductive apertures having an external surface in each of the flexible circuited substrates by having a first contact portion extending from the external surface of one flexible circuited substrate and a second contact portion extending substantially within both of the aligned conductive apertures thereby providing an electrical connection therebetween and mechanically securing the substrates together. The solder member not only electrically connects and mechanically unites the two flexible circuited substrates, it also acts as a connection point to chips on one circuited substrate and a connection point to a printed circuit board on the other circuited substrate.

Claim 44, as now presented, clearly sets forth these distinctions. Claim 44 now recites, for example, "at least one solder member including a first contact portion for

connection to a printed circuit board extending from said external surface of said conductive aperture of said first circuited substrate" (emphasis added). The Bindra, et al. arrangement is, in itself, a printed circuit board and thus cannot act as both a chip carrier that connects to a printed circuit board and a printed circuit board itself.

Claim 44 goes on to recite "a second contact portion extending substantially within both of said aligned conductive apertures of said first and second circuited substrates to said external surface of said conductive aperture of said second circuited substrate so as to substantially form a solder dome thereon to secure said circuited substrates together" (emphasis added). Bindra, et al. fail to teach or suggest any such solder dome structure which acts to provide both a contact point for a chip and as uniting structural support for holding the two circuited substrates together.

The Examiner has taken the position (e.g. Claim 39 rejection) in regard to the claim limitation calling for a solder dome that "Bindra, et al. further discloses that, *inherently by capillary action,* the second contact portion of solder member 2 is substantially in the form of a dome". However, Applicants have found no teaching in Bindra, et al. that supports the conclusion of the Examiner.

The dome-like structures shown in Fig. 4A of Bindra, et al. are stated, in col. 5, lines 60 - 66, to be "slight protrusions" formed "after joining metallization (2) has filled the vias (8) and cover the lands (7)" (emphasis added). The Bindra, et al. disclosure, at this point, goes on to state that "4B shows 4A after alignment, in the process of being joined and laminated to two additional circuited power cores (11) and (12), one on each major surface, the joining metal (2) to fill the vias (8) of the additional cores by capillary action".

The reference to "capillary action" in Bindra, et al. is thus made in regard to filling the vias of circuited power cores 11 and 12, similar to that shown in Figure 3D. There is nothing taught about such capillary action forming domes on circuited power cores 11 and 12 and nothing of this nature is shown in the drawings. In fact, Applicants do not understand how such capillary action could, indeed, form the solder domes claimed by Applicants. Clearly, the solder domes (2) shown in Fig. 4A and 4B are not taught by Bindra, et al. as being formed by capillary action but, in fact, are taught as providing a source of joining metal for the capillary action, itself. This would imply that the solder domes thus disappear after capillary action. Accordingly, they cannot, then, be made by capillary action.

There is also no teaching in Bindra, et al. of the Bindra, et al. solder structure acting to hold the circuitized power cones together. In fact, Bindra, et al. disclose in detail the process of laminating the power cores together.

Claim 44 goes on to recite "wherein said second contact portion of said solder member is at least one of an array of solder members on said external surface of said conductive aperture of said second circuited substrate" (emphasis added). Since Bindra, et al. teach nothing of solder domes in their aligned and assembled circuit board, as shown in Figures 3D and 4B, then it is not clear how the Examiner can conclude, as done in the rejection of Claim 40, for example, "that the second contact portion of solder member 2 is at least one of an array of solder members *inherently* on the *external (upper) surface*".

THE USC 103(a) REJECTION

The Examiner has rejected Claims 26 - 35 and 37 under 35 USC 103(a) as being unpatentable over Bindra, et al. in view of Crepeau and Casson, et al.

In brief, it is apparently the Examiner's position that Bindra, et al. discloses the claimed subject matter except for the flexible feature. In this regard, the Examiner states that "Bindra, et al. teaches that the first circuitized PTFE substrate of Fig. 4A and the second circuitized PTFE substrate 11 of Fig. 4B have a low dielectric constant (col. 2: 13 - 19) and are suitable for high temperature applications (col. 8: 35 - 38) but does not indicate that they are flexible structures".

The Examiner goes on to state that Crepeau discloses a stacked assembly of flexible circuitized substrates 14, 16 and 18 that are formed of TEFLON which is a PTFE material also having a low dielectric constant for the purpose of enhancing control over signal line impedance's (Figs. 1 and 2; col. 5: 20 - 26)".

In regard to Casson, et al., the Examiner states that the reference "discloses a stacked assembly of including flexible circuitized substrates formed of PTFE material suitable for high temperature applications, the flexibility of the circuitized substrates reducing mechanical stress on the substrate during operation (col. 14: 39 - 46; col. 16: 1 - 4 and 8 - 9; and col. 17: 24 - 27)". Applicants, however, find nothing in Casson, et al. in regard to the flexibility of the Casson, et al. PTFE material or to reducing mechanical stress by using PTFE in the Casson, et al. structure.

Crepeau is directed to a multilayer printed circuit board wherein flexible signal layers are positioned between a rigid component layer and another layer to form a rigid structure. The structure is mechanically held together by a nut and bolt arrangement.

Casson, et al. on the other hand, is directed to fabricating a heat resistant multilayer circuit board using an interconnecting adhesive layer comprising a conductive adhesive material having a plurality of deformable, heat fusible metallic particles dispensed

substantially throughout a non-conductive adhesive. In this regard, Casson, et al. state that (col. 14, line 35 et seq.) it is preferable to stack three double-sided circuit boards and interconnect them using layers of anisotropic conductive adhesive interposed therebetween". Casson, et al. go on to state that one advantage of this configuration is that heat resistant insulating substrates can be used on the outer layers, and less expensive heat sensitive insulating substrates can be use on the inner layers. Casson, et al. go on to state that the heat sensitive insulating substrates may be made of plastic materials such as polyethylene, polypropylene, polyethylene naphthalate, polyester, copolymers and combinations thereof. Applicants do not believe that latter qualify as PTFEs.

Thus, Crepeau and Casson, et al. are each directed to solving a different problem using different approaches to solving the problem. Crepeau is directed to forming a multilayer printed circuit board which can be readily disassembled. Casson, et al., on the other hand, is directed to forming a multilayer circuit board which is reliable, heat resistant and capable of withstanding thermal cycling. Casson, et al. achieve this by mechanically and electrically connecting together at least two conductive layers by an interconnecting adhesive layer.

Accordingly, Crepeau and Casson, et al. construct their multilayer printed circuit boards in a completely different manner resulting in quite different structures. Moreover, neither Crepeau nor Casson, et al. construct their multilayer printed circuit boards in any manner akin to the way Applicants construct their chip carrier electronic package. Neither reference teaches nor suggests anything whatsoever in regard to a chip carrier electronic package assembly having a pair of circuitized substrates which are both electrically and

mechanically connected together by a solder structure arrangement, as taught by Applicants.

More importantly, however, neither Crepeau nor Casson, et al. are at all akin to the teachings of the primary reference Bindra, et al. The Examiner states in paragraph VI that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the low dielectric PTFE material of Bindra, et al. with the flexible PTFE materials of Crepeau and Casson, et al.". In this regard, Applicants should point out the multilayer structural differences wherein Crepeau mechanically clamps the flexible layers together, Casson, et al. use adhesive to mechanically hold their layers together and Bindra, et al. laminate their layers together using temperature and pressure.

The Examiner states, in paragraph 1 of the 35 USC 103(a) rejection, that in Bindra, et al. "the first and second circuitized substrates are comprised of... (PTFE)" citing col. 6: 11 - 13 and col. 5: 62 - 66 of Bindra, et al. The Examiner has read the claimed second circuitized substrate on layer 11 in Fig. 4B of Bindra, et al. Applicants have not found any statement in Bindra, et al. that layer 11 is made of PTFE. The reference to PTFE (col. 6: 11 - 13) cited by the Examiner would seem to refer to layer 1 shown in Figures 2 and 3. See, for example, col. 7, lines 45 et seq. wherein the use of non-photosensitive material filled with PTFE is applied to the CPC's, as shown in Fig. 2A. Using this arrangement, Bindra, et al. employ lamination to apply the non-photosensitive material filled with PTFE to the CPC's. Thus, layer 11 of Bindra, et al., upon which the Examiner is reading the "second flexible circuitized substrate" limitation, does not appear to be PTFE, as asserted by the Examiner.

Accordingly, it is not at all clear how the teachings of Crepeau or Casson, et al. apply to Bindra, et al. Bindra, et al. are not concerned with flexible circuitized substrates, let alone PTFE type flexible substrates, as set forth in Applicants' claims. Applicants have not found where Bindra, et al. even mention flexible substrates, and it appears from the context of the Bindra, et al. description of CPC's and the various lamination steps, that Bindra, et al. involve quite the opposite.

Thus, Applicants not only fail to see how the teachings of either Crepeau or Casson, et al. apply to Bindra, et al., they also fail to see why one would want to modify Bindra, et al. with the use of the TEFLON of Crepeau, on the one hand, or the various PTFE materials suitable for high temperature applications of Casson, et al., on the other. Each of Crepeau and Casson, et al. are solving a different problem than Bindra, et al, and any incidental mechanical stresses incident thereto are handled in a manner unique to their assembled structure. In this regard, it is not at all clear whether modifying the low dielectric PTFE material used by Bindra, et al. by replacing it with the PTFE materials of Crepeau and Casson, et al. in order to reduce mechanical stress would, indeed, reduce stress. It may very well increase stress. In fact, it is not even clear whether Bindra, et al. would operate in the manner intended by Bindra, et al. if such modification were made.

Accordingly, Applicants believe that the Examiner's rejection of Claim 26 under 35 USC 103(a) on Bindra, et al., in view of Crepeau and Casson, et al. is in error for at least the reasons that:

- Bindra, et al. fail to describe the use of solder structure for mechanically and electrically connecting two flexible circuitized substrates together;
- Bindra, et al. do not teach using flexible circuitized substrates;

- Bindra, et al. describe PTFE in the context of a non-photosensitive material as a filled PTFE applied by to CPC's by lamination.

- There is no basis for combining Crepeau and Casson, et al. with Bindra, et al. since:

    - Bindra, et al. is directed to solving different problems than Crepeau and Casson, et al. resulting in different structures;

    - None of Crepeau, Casson, et al. or Bindra, et al. are explicitly directed to relieving mechanical stress;

    - Bindra, et al. form a laminate structure wherein flexible substrates do not necessarily offer stress relief.

Although Applicants believe that the Examiner's rejection of Claim 26 is in error, in order to expedite prosecution Applicants have amended Claim 26 to even more clearly define over Bindra, et al. As now set forth, Claim 26 not only recites a first and second flexible circuitized substrate, it also recites at least one solder member including "a first contact portion extending from said external surface of said conductive aperture of said first flexible circuitized substrate and a second contact portion extending substantially within both of said aligned conductive apertures of said first and second flexible circuitized substrates to said external surface of said conductive aperture of said second flexible circuitized substrate so as to substantially form a solder dome thereon and secure said flexible circuitized substrates together" (emphasis added). As pointed out by Applicants in regard to Claim 44, Bindra, et al. fail to teach or suggest any such solder dome structure on a second circuitized substrate and there is no teaching or suggestion of achieving this by capillary action. In fact, it is not clear that capillary action could produce such a dome structure.

As to the Examiner's rejection of dependent Claims 28 and 29, notwithstanding the Examiner's column and line references to Bindra, et al., Applicants have not found specific teachings in modified Bindra, et al. as to the temperature and materials specified in these claims.

As to the Examiner's rejection of Claim 30, the solder member 2 of Bindra, et al., as previously discussed in regard to the solder dome limitation, acts as a source of joining metal upon assembly and, thus, disappears. Accordingly, it cannot meet the recitation calling for a solder member having a "cross-sectional configuration that is substantially round, oval, or ellipsoidal".

As to the Examiner's rejection of Claim 31 on modified Bindra, et al., contrary to the Examiner's assertions, layer 12 of Bindra, et al. is not a printed circuit board. In column 5, lines 62 - 66, Bindra, et al. defines layers 11 and 12 as circuitized power cores. These power cores go to make up a laminated printed circuit board and, thus, cannot be a distinct and separate printed circuit board to which a chip carrier electronic package is attached. The chip carrier electronic package recited in the claims has a solder member extending from the external surface of said first flexible circuitized substrate to connect to a separate printed circuit board.

The Examiner has rejected Claims 32 and 33 on modified Bindra, et al. based upon the assertion that Bindra, et al. "discloses that the second contact portion of the solder member 2 extends *inherently by action* at least to the external (upper) surface of the conductive aperture metallization of the circuitized substrate 11" and "is inherently (also by capillary action) in the shape of a dome". As previously pointed out by Applicants', the relevant description in Bindra, et al., col. 5, lines 49 - 57, states that solder "enters the vias

in the female CPC by capillary action" and, col. 5, lines 65 - 66, states "the joining metal (2) to fill the vias (8) of the additional cores by capillary action". Nothing is stated in regard to forming domes by capillary action and Applicants really do not understand how such would inherently be formed by capillary action. The relevant description in Bindra, et al. in regard to domes (2) can be found in col. 5, lines 35 - 39 wherein it is stated that Figure 3B "shows 3A after dielectric material (10), such as photoresist, has been applied and the vias (8) and lands (7) have been opened up and filled with joining metal (2)". Thus, the domes (2) are formed by filling prior to any subsequent capillary action and, as pointed out previously, in fact act as a source of material for the subsequent capillary action.

Accordingly, since the limitations of canceled Claims 32 and 33 have been incorporated into parent Claim 26, then Claim 26, for the above reasons, further distinguishes over Bindra, et al. In addition, rejected Claim 35, dependent upon Claim 34, therefore also distinguishes over Bindra, et al. Similarly, rejected Claims 36 and 37, dependent upon patentably distinct Claim 26, are also allowable.

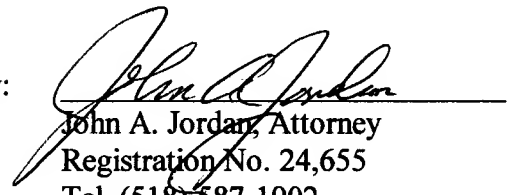
Attached hereto is a marked-up version of the changes made to Claims 26, 34 and 44. The attached page is captioned **"VERSION WITH MARKINGS TO SHOW CHANGES MADE"**.

Accordingly, in view of Applicants' amendment to the claims and remarks, Applicants firmly believe the case is now in condition for allowance. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw his rejections,

allow the case as now presented and pass the case to issue.

Respectfully submitted,

Gregg J. Armezzani, et al.

By: 

John A. Jordan, Attorney
Registration No. 24,655
Tel. (518) 587-1902

RAK/JAJ